IN THE SPECIFICATION

Please replace the title on page 1 line 1 with the following:

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING PLURAL MEMORY CIRCUITS SELECTIVELY CONTROLLED BY A MASTER CHIP ENABLE TERMINAL OR AN INPUT COMMAND AND OUPTTING A PASS/FAIL RESULT

Please replace the paragraph beginning at page 1, line 26, with the following rewritten paragraph:

Such a waiting time in the busy state of the EEPROM flash memory adversely affects the high-speed performance of a memory system. Therefore, in order to realize a high-speed performance in a flash memory system using a plurality of memory chips, it is effective to commonly use a data bus for time-sharing inputting commands and data to carry out internal operations in the plurality of memory chips in parallel. The inventors have proposed such a technique (Japanese Publication (Kokai) Nos. ~~6-95125 and 6-95126~~ 07-302175 and 07-302176, US Patent No. 5,603,001, etc.).

Please replace the paragraph beginning at page 2, line 8, with the following rewritten paragraph:

As circumstances on the side of a Central Processing Unit (CPU) for controlling a memory system, there are also circumstances wherein even if the storage capacity of a required memory system increases, the size of a handled file other than image files often does not remarkably increase, and many small-size files are rather preferably handled. The page mapping size of the CPU of personal computers is also maintained to be, e.g., 4 kilobytes, as a common value regardless of the generation of the CPU.

Please replace the paragraph beginning at page 3, line 14, with the following rewritten paragraph:

According to the present invention, a plurality of memory circuits (EEPROM circuits) in a single chip can be operated in time sharing or in parallel as if ~~plurality~~ plural chips are operated. Therefore, unlike a case where the storage capacity of a single chip is simply increased by a single control circuit, even if a certain circuit is in a busy state, it is possible to access other memory circuits, so that it is possible to obtain a high-speed performance memory system without waiting time at sight from the outside.

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Please replace the paragraph beginning at page 4, line 28, with the following rewritten paragraph:

FIG. 2 shows the construction of each of the EEPROM circuits 2. A memory cell array 21 has electrically rewritable nonvolatile memory cells which have a stacked gate structure and which are arranged and connected so as to form a NAND type. The word and bit lines of the memory cell array 21 are selected by a row decoder 22 and a column decoder 25, respectively. An address signal is incorporated into an address register 27, via an input/output (I/O) buffer, 26 to be decoded by the row decoder 22 and the column decoder 25 to select a memory cell. The bit lines of the memory cell array 21 are connected to a sense amplifier 23 which is connected to the I/O buffer 26 via a data register 24.

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Please replace the paragraph beginning at page 5, line 2, with the following rewritten paragraph:

In order to generate various high voltages for use in data writing and erasing, a booster power supply circuit 30 is provided. A control circuit 29 is designed to sequentially control data writing and erasing including verify operations, and simultaneously control the booster power supply circuit 30 in accordance with an operation mode. A command CMD for writing or erasing is incorporated into a command register 28 via the I/O buffer 26. The command incorporated into the command register 28 is decoded by the control circuit 29 to control writing or erasing in accordance with the command. Various enable signals including

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enable signals /CE, which are input to the chip enable terminals CE and which are indicative of the activity and inactivity of the whole circuit, enter the I/O buffer 26. ~~These~~ The enable signals are also fed to the control circuit 29. The control circuit 29 outputs a busy signal to the terminal R/B via a Ready/Busy buffer 31 when the enable signal /CE = H.

Please replace the paragraph beginning at page 5, line 22, with the following rewritten paragraph:

As described above, according to this preferred embodiment, a plurality of EEPROM circuits having an autonomous control function are provided in a single chip, so that it is possible to operate the EEPROM circuits in parallel to carry out a high-speed operation of a large-capacity memory. Each of the EEPROM circuits is provided with a chip enable terminal and a Ready/Busy terminal corresponding thereto, so that it is possible to control each of the EEPROM circuits from the outside as an independent memory chip. Therefore, unlike a case where the storage capacity of a single chip is simply increased, it is possible to realize a high-speed performance, and it is possible to flexibly cope with a request for inputting/outputting ~~by small unit of storage capacitor~~ data for every small unit of storage capacity.

Please replace the paragraph beginning at page 7, line 18, with the following rewritten paragraph:

It is assumed that [[a]] the memory function register 4 is controlled by inputting a command. For example, when the chip enable CE is activated to input a command to indicate that the chip enable terminal CE1, i.e., the EEPROM circuit 2-1, is selected, the memory function register 4 causes the chip enable CE to be enabled with respect to the EEPROM circuit 2-1. At this time, the Ready/Busy terminal R/B outputs the Ready/Busy state of the EEPROM circuit 2-1. When the chip enable CE is deactivated, the chip enable with respect to the whole memory chip 1b is negated.

Please replace the paragraph beginning at page 7, line 28, with the following rewritten paragraph:

If access sorting is thus carried out with respect to the plurality of EEPROM circuits in the memory chip, it is possible to control a large-capacity memory system by the same number of signal terminals as that in the case of a single EEPROM circuit. Therefore, the same CPU can be connected to any one of a number of memory chips, the generations of which are different, by only the change of a software.

Please replace the paragraph beginning at page 7, line 35, with the following rewritten paragraph:

When the chip enable signal CE is deactivated, ~~the control is not often continued for each of the EEPROM circuits~~ it is seldom that each EEPROM circuit is controlled continuously. Therefore, if the selection to each of the EEPROM circuits is released in connection therewith, the release of the selection can be easily controlled, and the subsequent control can be easily carried out.

Please replace the paragraph beginning at page 8, line 27, with the following rewritten paragraph:

According to such a preferred embodiment, it is not required to scan the signal terminals in order to monitor the Ready/Busy signal of each of the EEPROM circuits. Therefore, it is also not required to estimate a delay in switching transition time, such as a case where the same signal line is switched to output the Ready/Busy signal of each of the EEPROM circuits. Moreover, if a command control can acquire the Ready/Busy states of the respective EEPROM circuits at [[a]] one time, it is possible to carry out [[one]] a high-speed operation control.

Please replace the paragraph beginning at page 9, line 11, with the following rewritten paragraph:

FIG. 7 shows another preferred embodiment of a memory chip ld according to the present invention. In this preferred embodiment, an area selecting decoder 6 for selecting one of EEPROM circuits 2, which is to be written/erased, in response to an inputted command is provided in the memory chip ld between a common data bus 3 for the EEPROM circuits 2 and an external I/O terminal. This area selecting decoder 6 allows commands, addresses and data to be inputted to the I/O buffer of each of the EEPROM circuits 2 in time sequence. In this case, it is assumed that it is possible to optionally set the order in which the EEPROM circuits should be selected. Each of the EEPROM circuits 2 does not include ~~any control circuits and a~~ controllers of command, address, and data. A single control circuit 7 for controlling writing or the like in the EEPROM circuits 2 is provided.

Please replace the paragraph beginning at page 11, line 4, with the following rewritten paragraph:

In this preferred embodiment, it is preferably possible to select one of a mode, in which the next data are inputted to the data buffer after referring to the Pass/Fail result of data writing, and a mode, in which data are continuously inputted to the data buffer without referring to the Pass/Fail result. In this case, the meaning of how to output a Busy signal is different in the respective modes. That is, in the former mode, it is assumed that the Busy state is completed when the state of the written result can be referred. In this case, since the data writing is actually completed, the next data can be input. In the latter, it is assumed that the Busy state is completed when the next data writing can be carried out.

Please amend the Abstract on page 15 as follows:

ABSTRACT OF THE DISCLOSURE

A nonvolatile semiconductor memory device capable of controlling a single memory chip similar to a plurality of memory chips. The memory chip has a plurality of ~~Electronically~~ Electrically Erasable Programmable Read Only Memory circuits, each of

which includes a control circuit for carrying out sequential writing control and which EEPROM circuits share a data bus. Each of the EEPROM circuits has a Chip Enable terminal CE and a Ready/Busy terminal R/B, so that data writing processes can be simultaneously carried out in the respective EEPROM circuits in parallel. The activity and

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inactivity of each of the EEPROM circuits may also be controlled by a logical combination of a master chip enable signal and a chip enable signal of each of the individual EEPROM circuits. A pass or fail result of writing operations may be output or held and accumulated, with the nonvolatile semiconductor memory device having modes of operation in which it is determined whether data may be input to a data buffer by selectively referring to a pass/fail result.